Workshop on Knowledge Discovery in Scientific Apllications
17-19 listopad, 2008, Poreč

Applied scientific research with industrial impact

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Laboratorij za istraživanje slučajnih signala i procesa

Mjerno analitička proceduralna tehnologija za mjerno-senzorske i/ili komunikacijske primjene u elektronici i optoelektronici

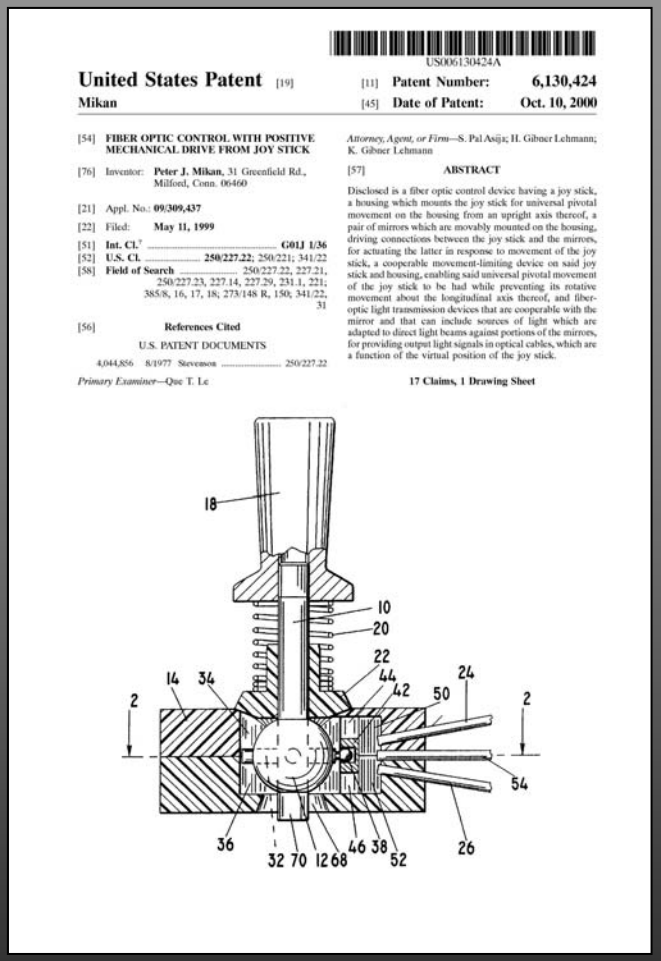
- Suvremena znanstvena mjerna instrumentacija
- Virtualna mjerna instrumentacija (LabVieW + National Instuments DAQ)

- Programirljiva logička tehnologija

- MentorGraphics
- MatLab
- MATEMATICA
- Statistica, Origin

Istraživačka problematika iz područja optoelektronike

- Optoelektronički detektor položaja šipki izvora radioaktivnog zračenja (1983)
- Mjerenje značajki optičkih vodova (Iskra, 1991)
- Time-of-flight laserski sustavi (1993)
- Svjetlovodni senzor doze gamma zračenja (1996)
- Kvantni generator slučajnih brojeva (WB, 2004)
- Optimalizacija optičkog joysticka (SAD, 2007)
- ELKA – tvornica optičkih kabela (2008) ?



US006130424A

United States Patent [19]
Mikan

[11] **Patent Number: 6,130,424**
[45] **Date of Patent: Oct. 10, 2000**

[54] **FIBER OPTIC CONTROL WITH POSITIVE MECHANICAL DRIVE FROM JOY STICK**

[76] Inventor: **Peter J. Mikan**, 31 Greenfield Rd., Milford, Conn. 06460

[21] Appl. No.: **09/309,437**

[22] Filed: **May 11, 1999**

[51] **Int. Cl.**[7] **G01J 1/36**
[52] **U.S. Cl.** **250/227.22**; 250/221; 341/22
[58] **Field of Search** ..... 250/227.22, 227.21, 250/227.23, 227.14, 227.29, 231.1, 221; 385/8, 16, 17, 18; 273/148 R, 150; 341/22, 31

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,044,856 8/1977 Stevenson 250/227.22

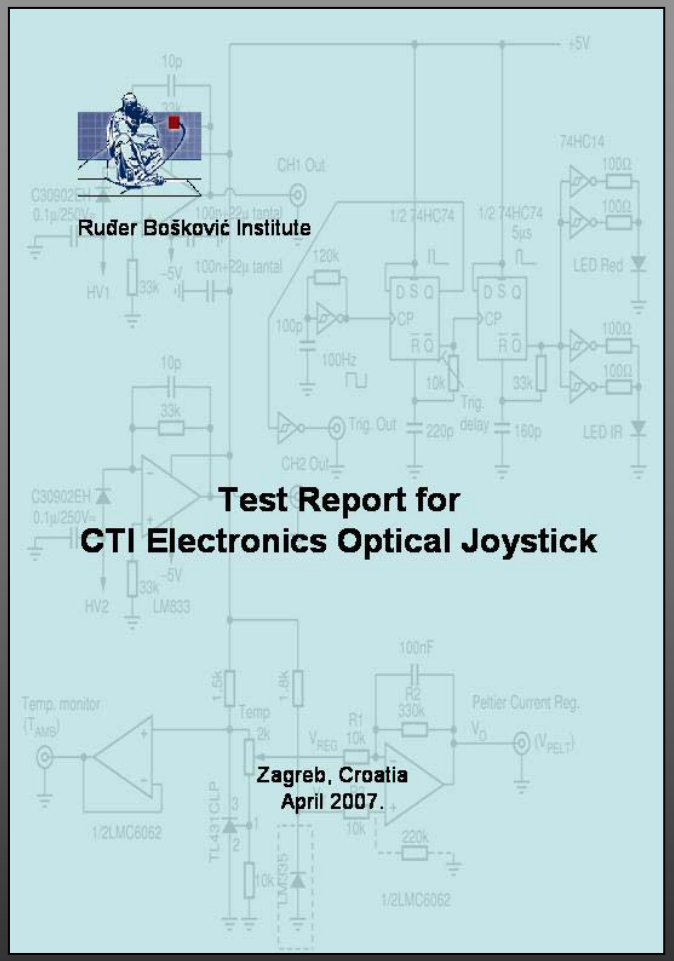
Primary Examiner—Que T. Le

Attorney, Agent, or Firm—S. Pal Asija; H. Gibner Lehmann; K. Gibner Lehmann

[57] **ABSTRACT**

Disclosed is a fiber optic control device having a joy stick, a housing which mounts the joy stick for universal pivotal movement on the housing from an upright axis thereof, a pair of mirrors which are movably mounted on the housing, driving connections between the joy stick and the mirrors, for actuating the latter in response to movement of the joy stick, a cooperable movement-limiting device on said joy stick and housing, enabling said universal pivotal movement of the joy stick to be had while preventing its rotative movement about the longitudinal axis thereof, and fiber-optic light transmission devices that are cooperable with the mirror and that can include sources of light which are adapted to direct light beams against portions of the mirrors, for providing output light signals in optical cables, which are a function of the virtual position of the joy stick.

17 Claims, 1 Drawing Sheet

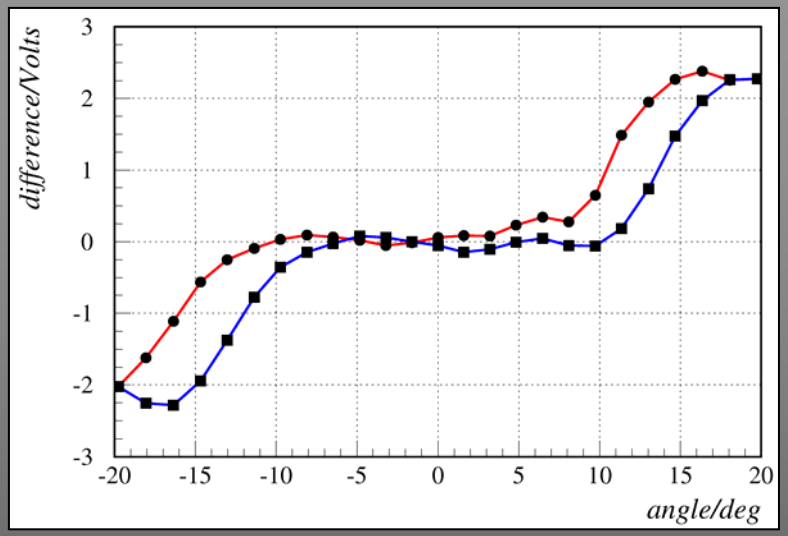


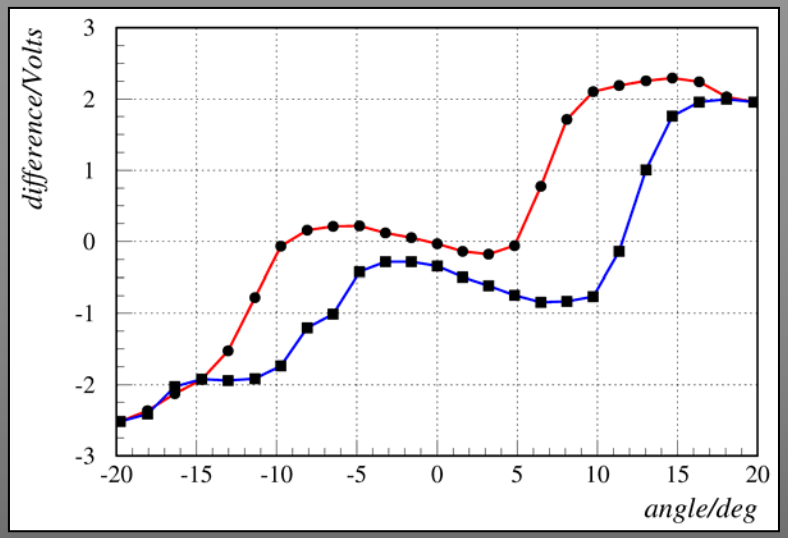
Branka Medved Rogina, Peter Škoda (ZEL)
Mario Stipčevoć (ZEF)

Test report for CTI Electronics optical joystick

The aim of the project is to experimentally establish the base line of CTI Electronics optical joystick performance and explain the main features of its response in order to be able to address solutions for improving the performance.

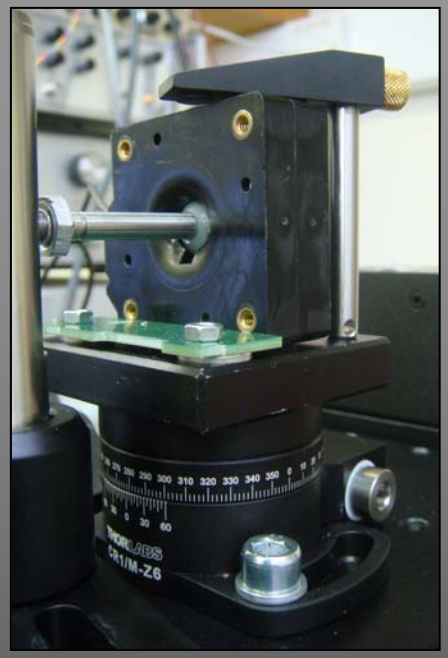
The measurements of joystick response characteristics were made thought the development of LabVIEW application program and the assembly of mechanical translation stage and electronics hardware circuitry. Through these means, alterations of joystick response characteristics due to movement of joystick lever and functional differences in detection channels (reflective mirrors) have been quantified.



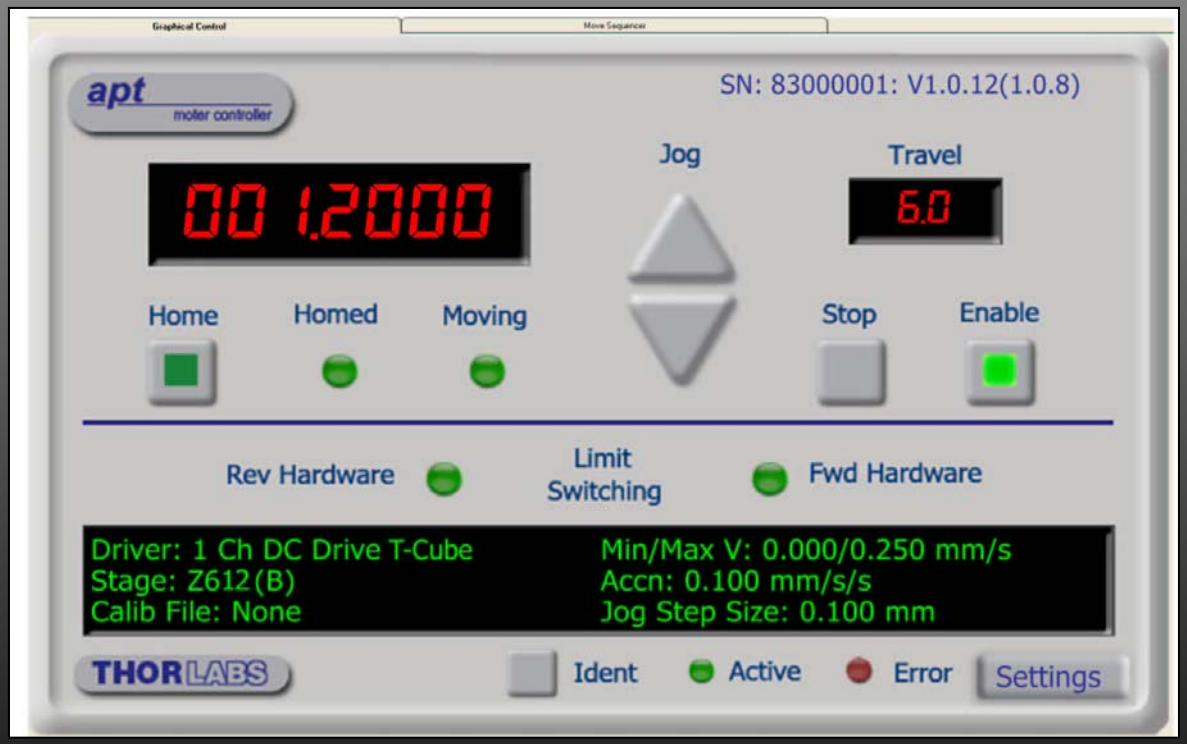


In accordance to the above, we have defined the list of tasks to be done:

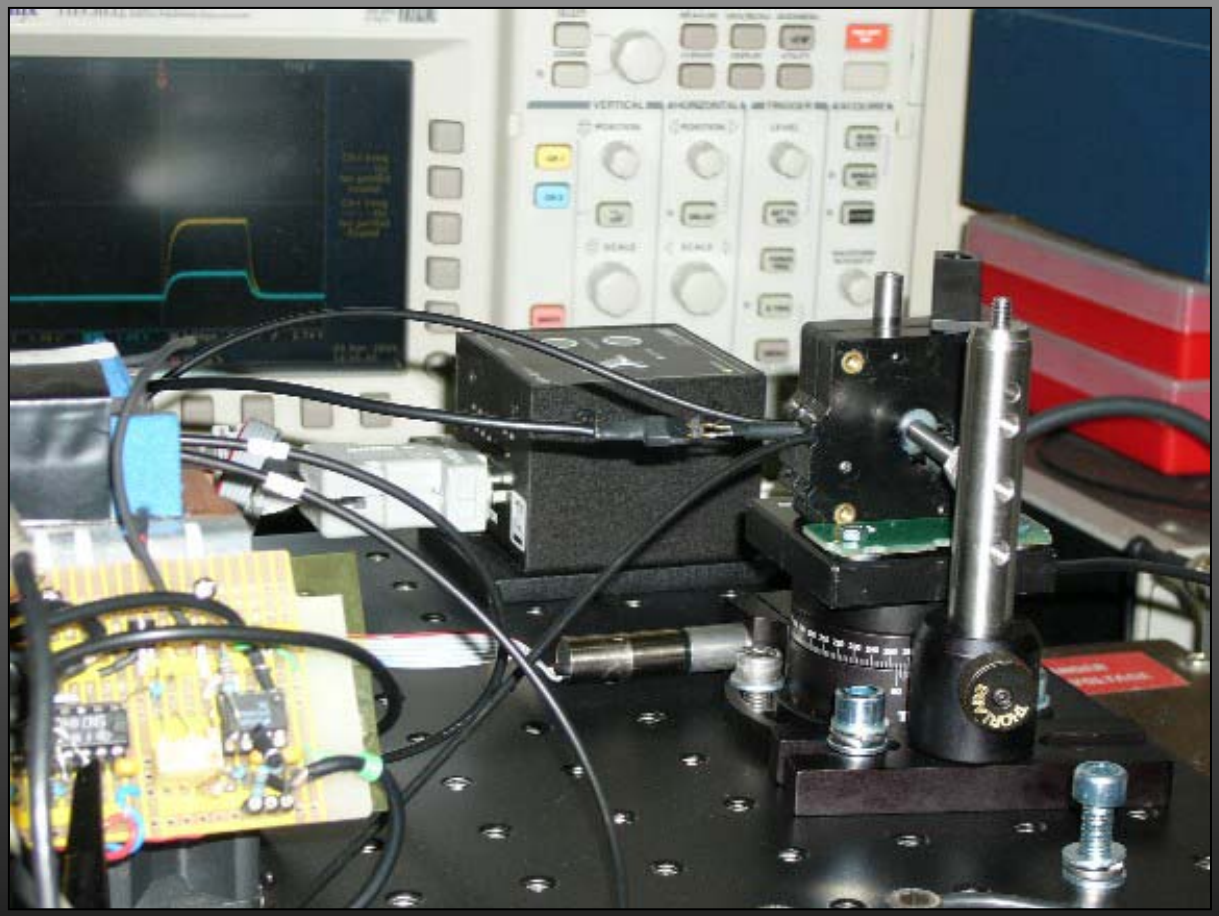
- to determine the best way to improve the linearity and the efficiency of the output voltage(s) with respect to the said movement;
- to investigate a possibility to make the plateau regions smaller with respect to the active response area.
- to find a way to perform adjustment of the light intensity of the source such that the voltage span at the output is independent of aging, temperature effects etc.



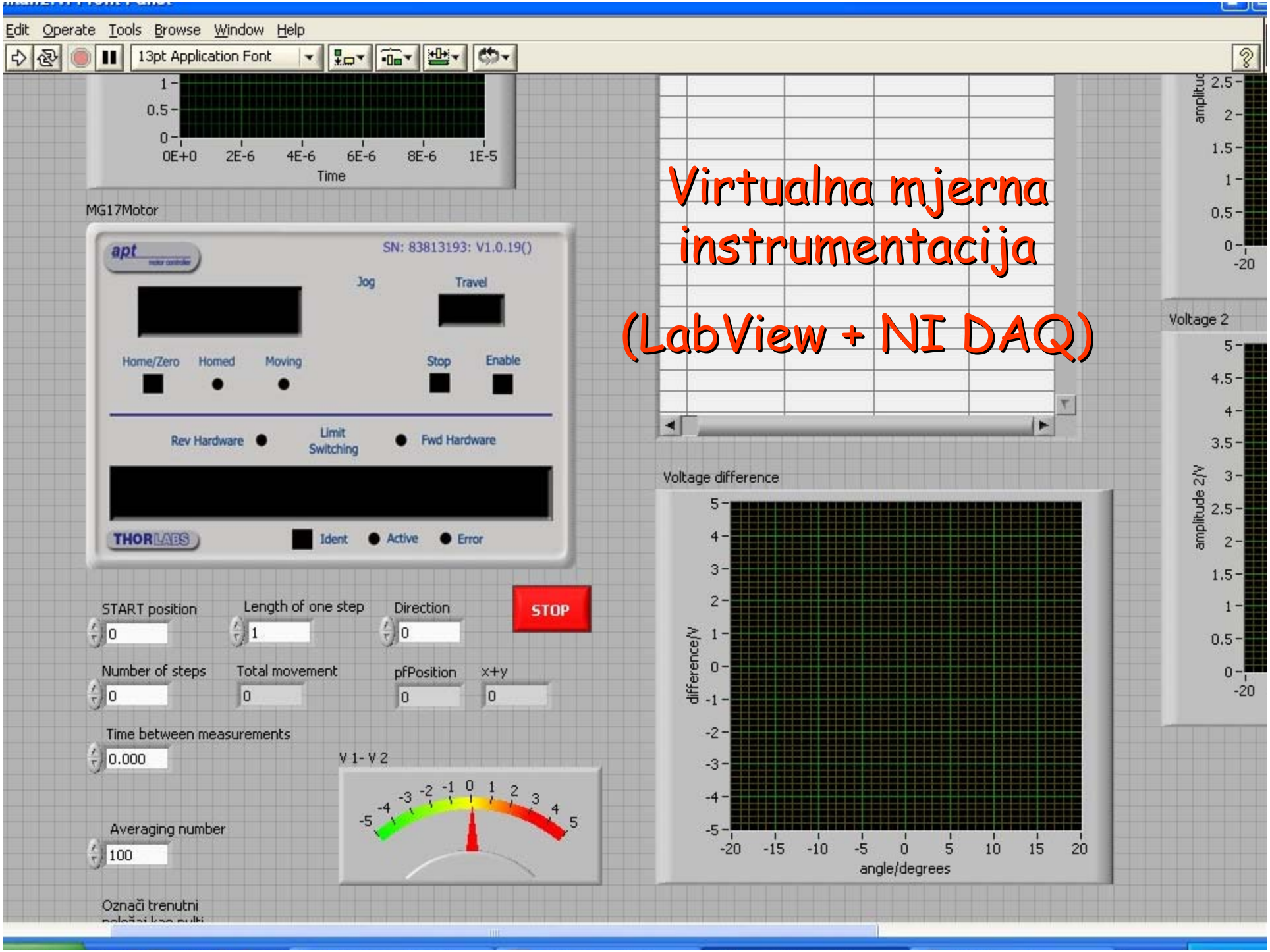
Motorized rotation stage CR1/M-Z6E with driver (Thorlabs)

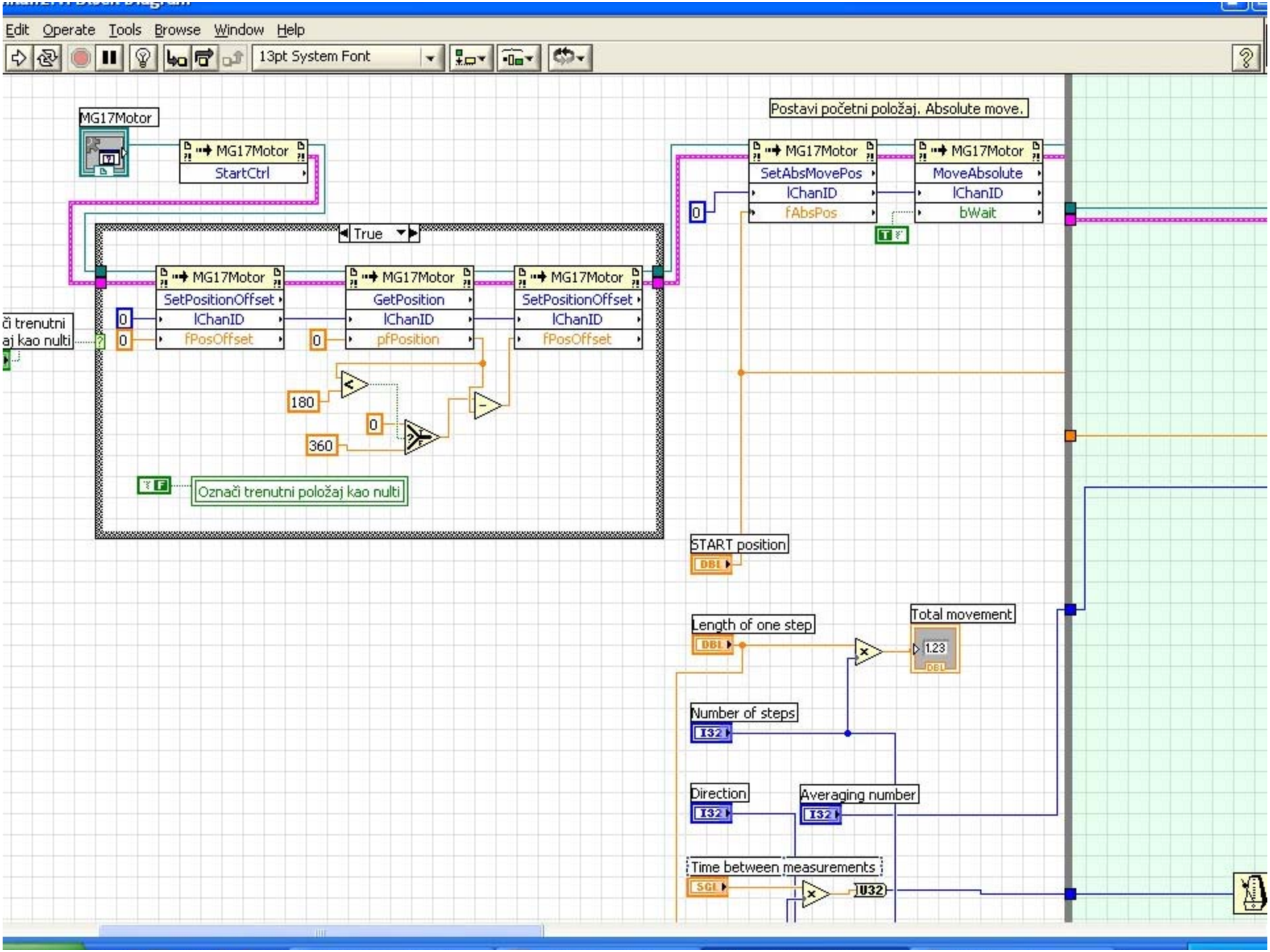


Postav za automatizirano, pozicijski razlučeno (x,y) mjerenje vrlo niske razine svjetla_ver. 2



Virtualna mjerna instrumentacija (LabView + NI DAQ)




Edit Operate Tools Browse Window Help
13pt System Font
MG17Motor
MG17Motor
StartCtrl
Postavi početni položaj. Absolute move.
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fAbsPos
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fPosOffset
MG17Motor
GetPosition
lChanID
pfPosition
MG17Motor
SetPositionOffset
lChanID
fPosOffset
180
360
Označi trenutni položaj kao nulti
START position
Length of one step
Total movement
Number of steps
Direction
Averaging number
Time between measurements

Mikan2_v2a_BMR.vi
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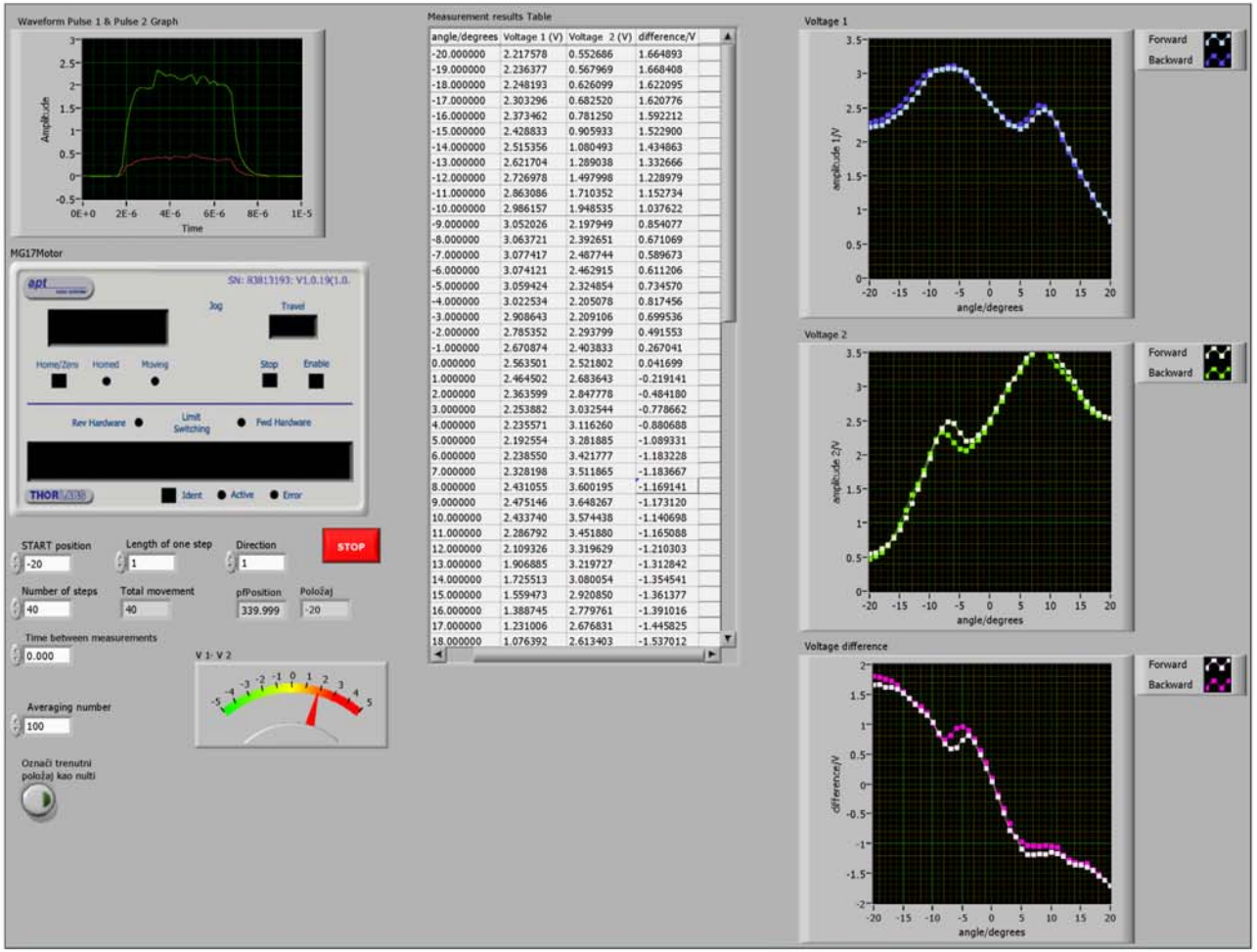
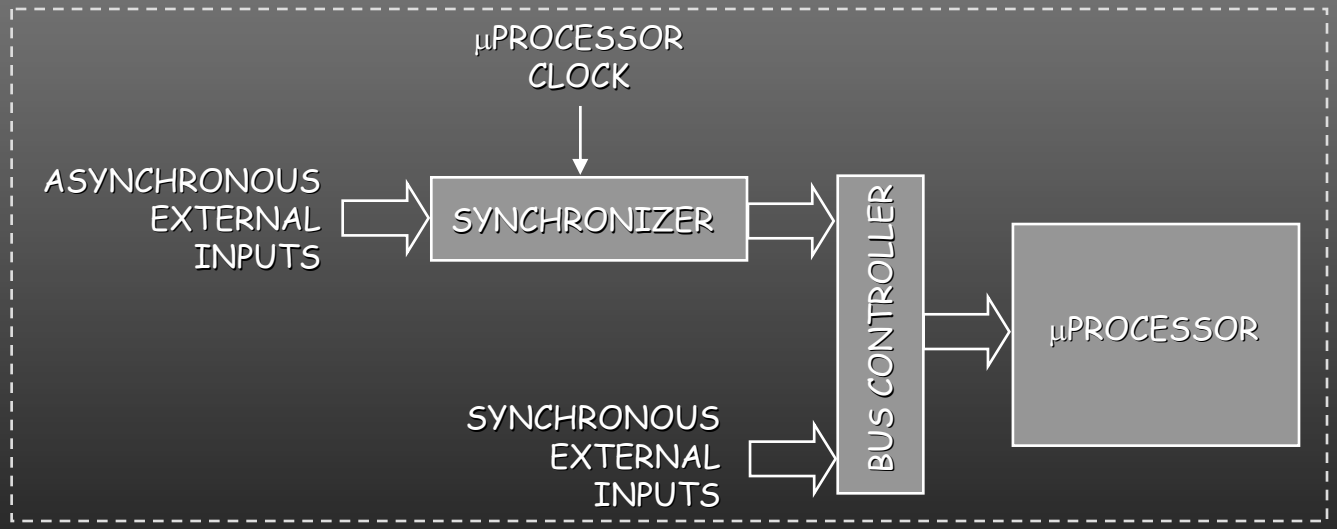
Last modified on 8.7.2008 at 16:51
Printed on 12.8.2008 at 13:51

Front Panel

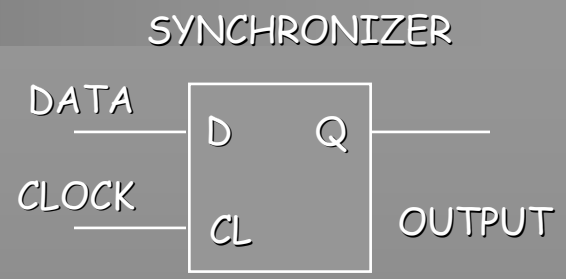


Vremenske značajke VLSI logičkih sklopova (mjerenje kratkih vremenskih intervala)

- globalno asinhroni i lokalno sinhroni sustavi
- gustoća integracije i brzina rada se povećavaju: zahtjevi na vremenske značajke i sinkronizaciju

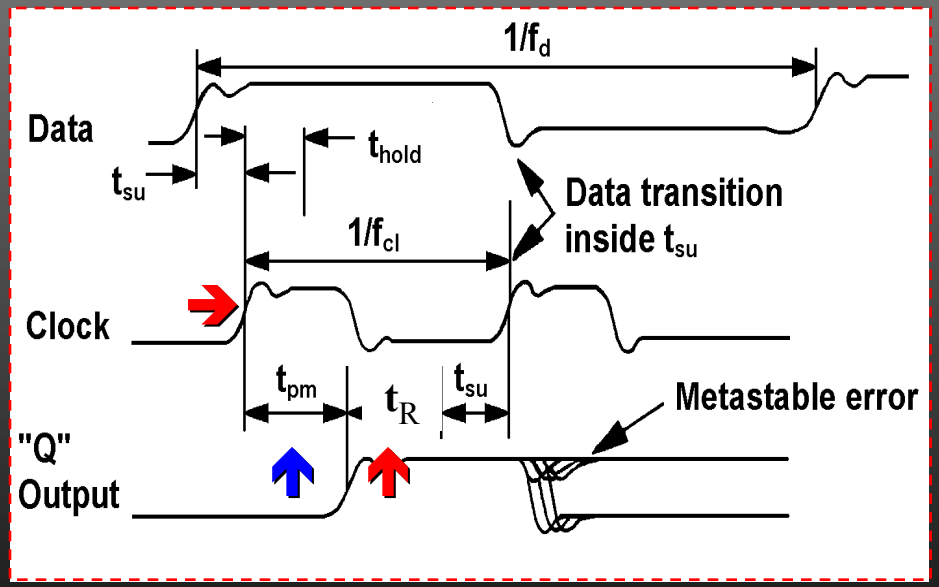


D bistabil: memorijski element

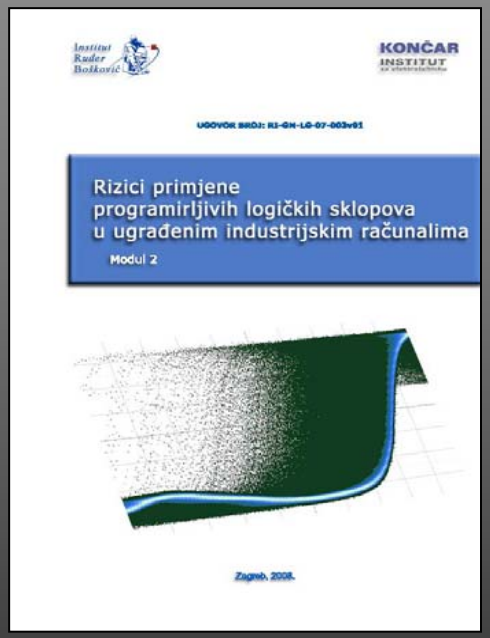


- Asinhroni ulazni signali koji ne zadovoljavaju vrijeme postavljanja i vrijeme zadržavanja dovode do metastabilnosti
- Povećanje respoloživog vremena smirivanja rezultira ukupnim povećanjem vremena kašnjenja flip-flopa
- Pogreška nastaje AKO se izlaz nije ustalio do trenutka kada postaje ulazni signal za sklopovlje koje slijedi

$$t_R = \left(1/f_{CL} - t_{PD} - t_{SU}\right)$$



Rizici primjene programirljivih logičkih sklopova u ugrađenim industrijskim računalima



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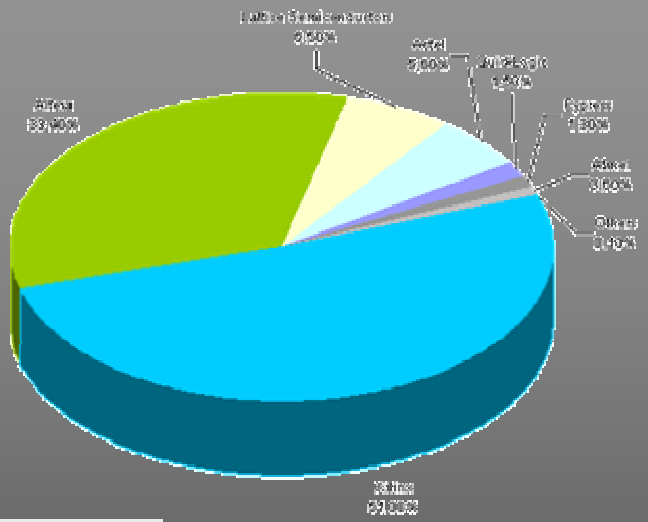
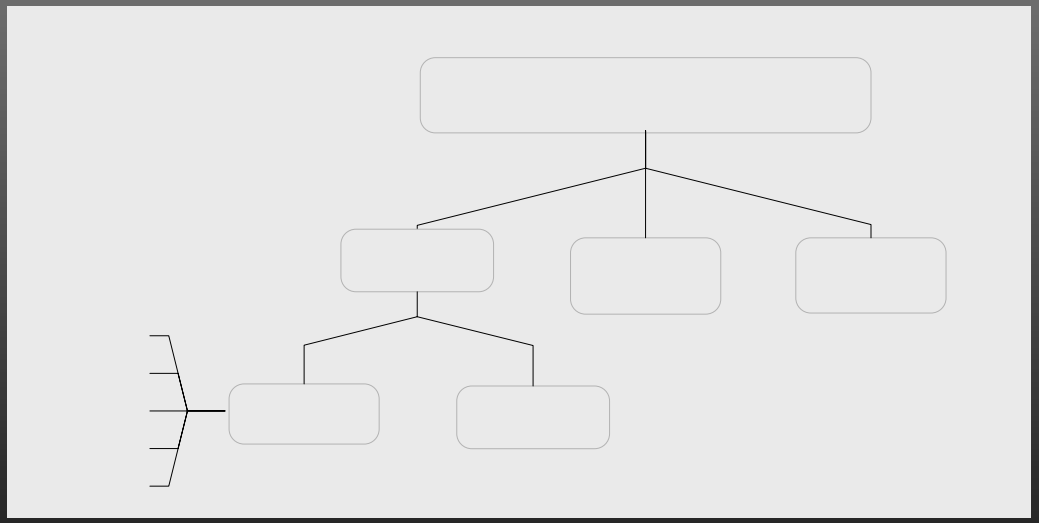
Maja Vlah, Siniša Marijan – IET Končar

Programirljivi logički sklopovi

- Digitalni integriranih logički sklopovi koji se mogu konfigurirati za izvršenje željene funkcije, a prema specifičnim namjenski određenim zahtjevima.
- Konfiguriranje programirljive logičke strukture se postiže putem namijenskih programskih alata koji korisniku pomažu definirati željenu funkciju sklopa.
- Na taj način upotreba programirljive tehnologije pruža inženjerima veću fleksibilnost i kraće vrijeme potrebno za razvoj, testiranje i implementaciju sklopovske izvedbe.
- Raspon funkcija koje ovi sklopovi mogu izvršavati je prilično širok: od jednostavnih, poput dekodiranja adresa, do vrlo složenih, poput mikrokontrolerskih sustava.

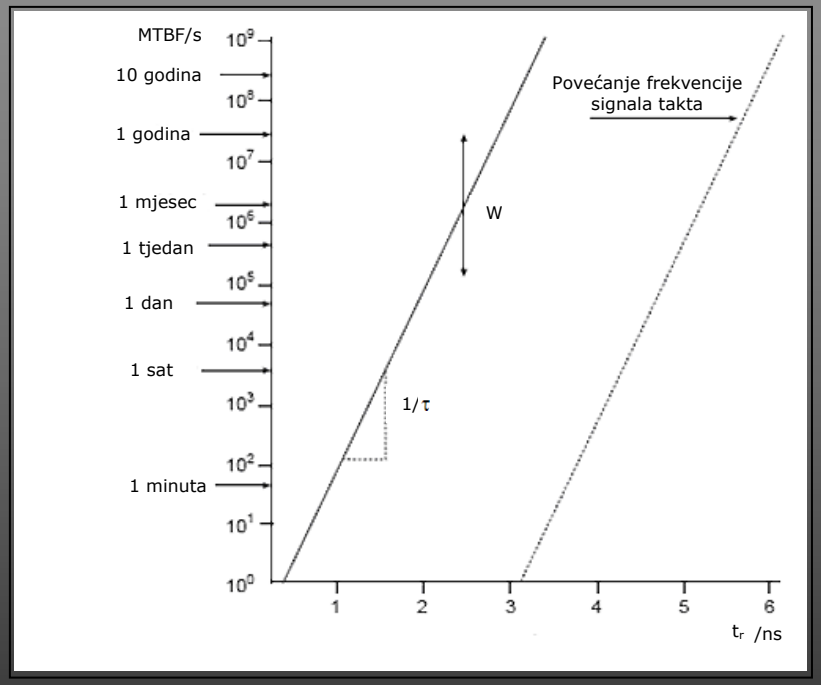
Podjela programirljive logike





Jednadžba metastabilnosti

Kolika je vjerojatnost da će sklop ući u metastabilnost?
Koliko dugo će to stanje trajati?



$$MTBF = \frac{e^{\frac{t_R}{\tau}}}{2 \cdot f_{CL} \cdot f_D \cdot W} \; ili \; \frac{10^{\frac{t_R}{\tau_D}}}{2 \cdot f_{CL} \cdot f_D \cdot W}$$

f_{CL} frekvencija clocka
f_D frekvencija podataka
W prozor metastabilnosti (vjerojatnost ulaska u metastabilnost!)
t_R raspoloživo vrijeme smirivanja
τ konstanta razlučivosti (vrijeme trajanja metastabilnosti!)
τ_D $= \tau/\log(e)$

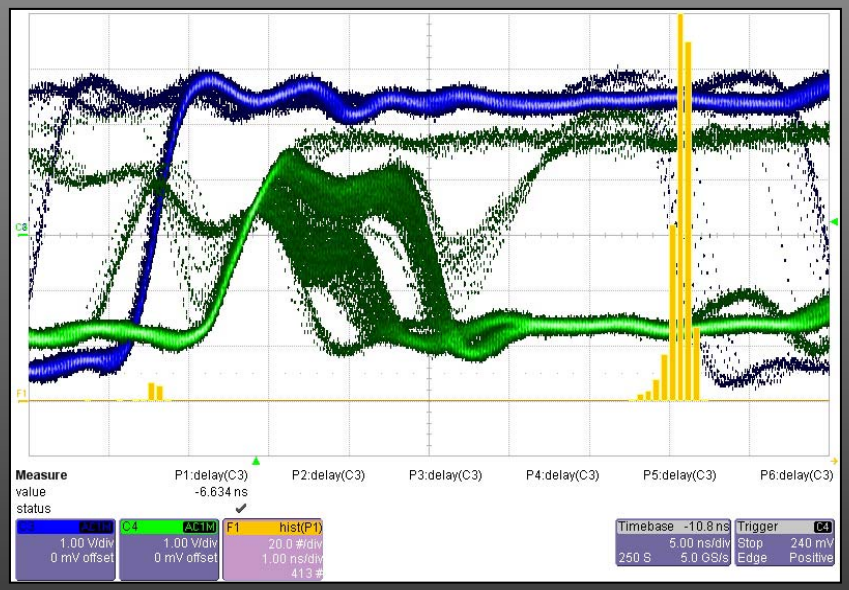
Mjerne metode

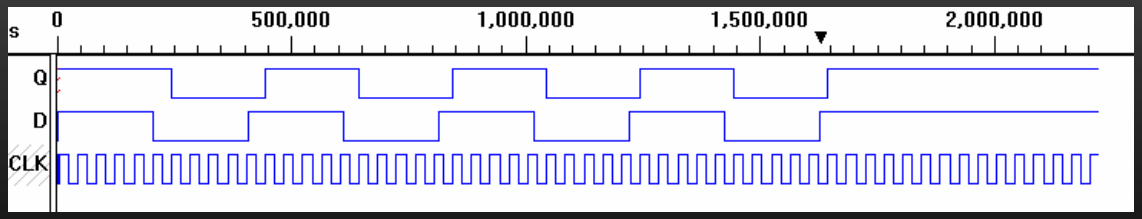
Metoda inicirane metastabilnosti sinkronim signalima pobude (Foley)

Metoda inicirane metastabilnosti asinkronim signalima pobude (oscilatori)

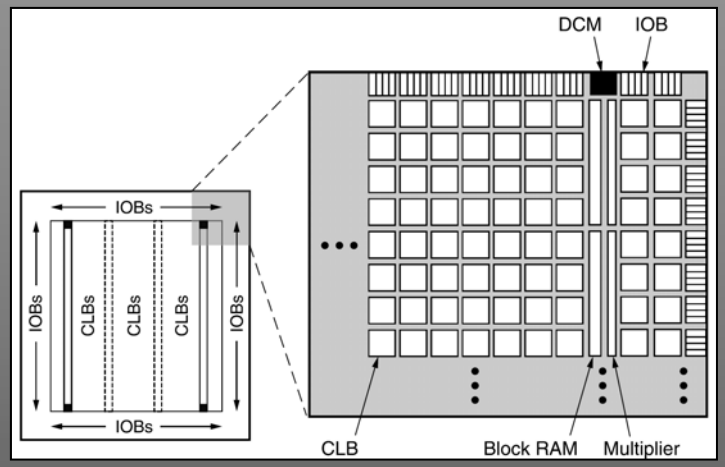
Late transition detection (LTD) metoda

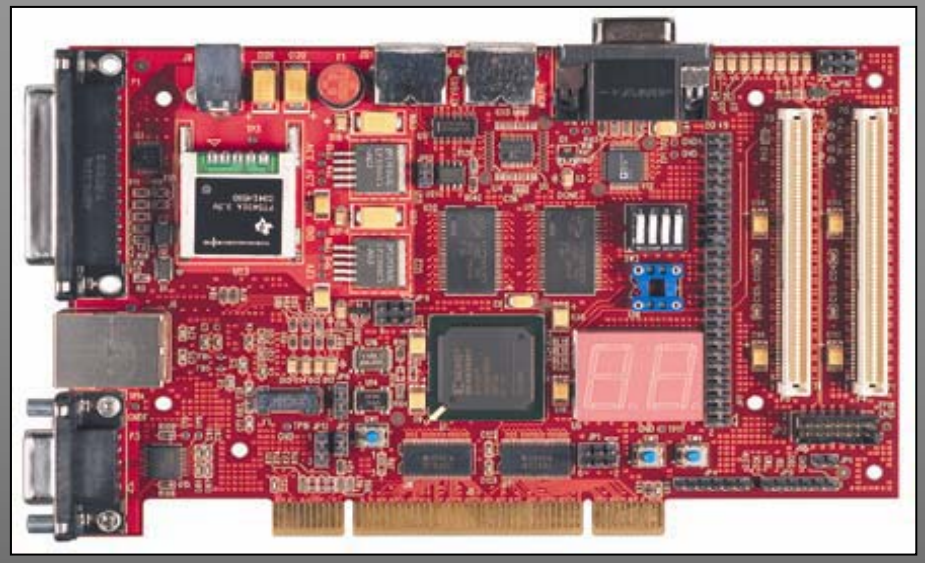
ispMACH 4A (PLD)





Spartan-3





Configurable Logical Block (CLB) – logički blokovi koji sadrže pregledne tablice (Look-Up Table – LUT) kojima se ostvaruju logičke funkcije

Input/Output Block (IOB) – ulazno/izlazni blokovi kojima se prenose podaci između I/O izvoda i interne logike.

Block RAM (BRAM) – memorijski blokovi, veličine 18 kbit koji se mogu spajati u memorije željenog kapaciteta i širine riječi.

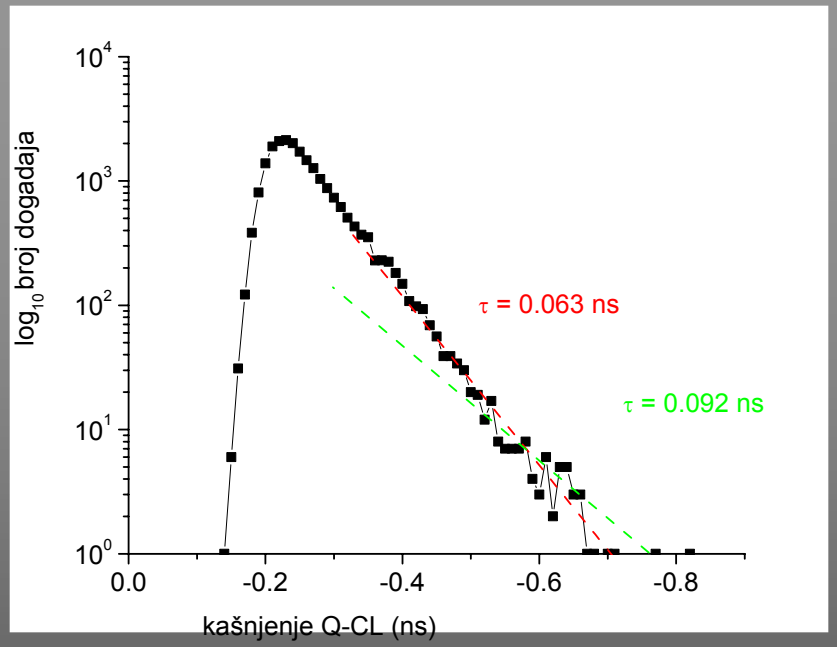
Multiplier Block – 18x18-bit množila.

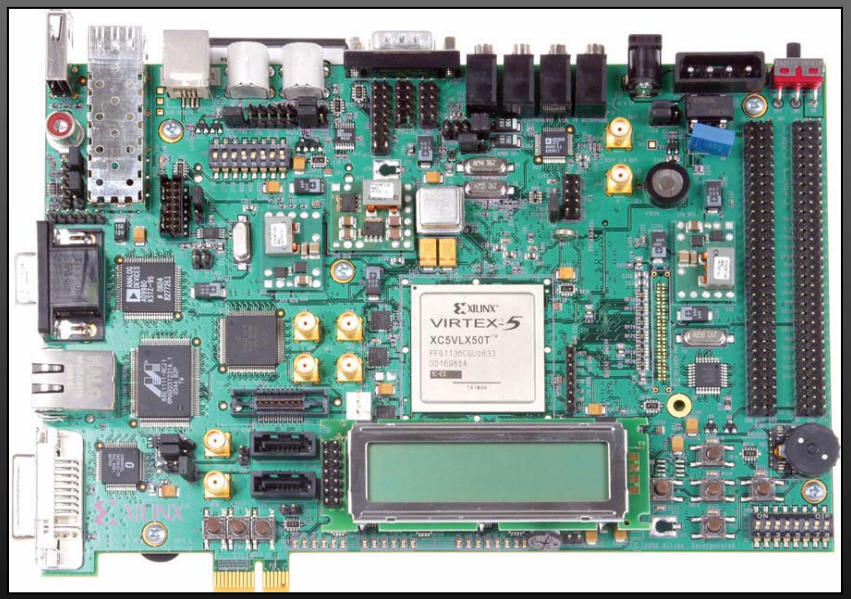
Digital Clock Manager (DCM) Block – blokovi namijenjeni distribuciji, kašnjenju, djeljenju, množenju i faznom pomicanju signala takta.

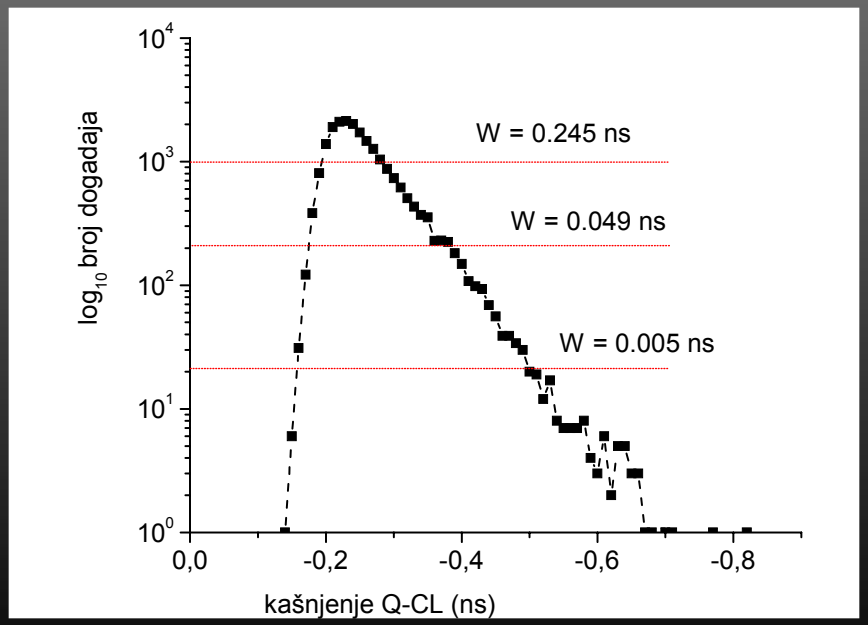
0.8 – 2.31 ns vrijeme kašnjenja
5.18 ns vrijeme postavljanja
3.57 ns vrijeme zadržavanja

Virtex-5

Phase Locked Loop (PLL) Block, Digital Clock Manager (DCM) Block – elementi namijenjeni generiranju i distribuciji signala takta.
Embedded Processor Block – PowerPC 440 procesor

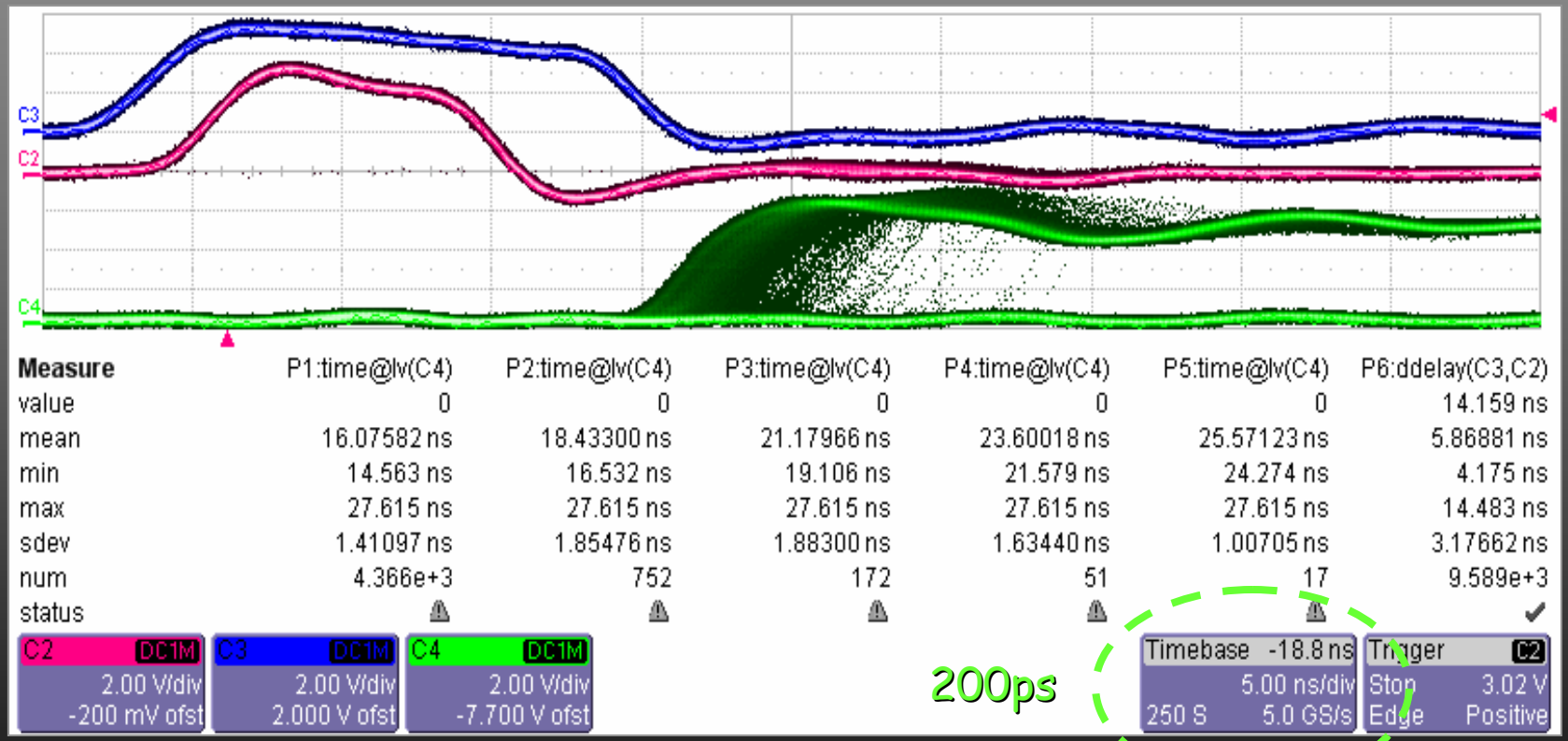






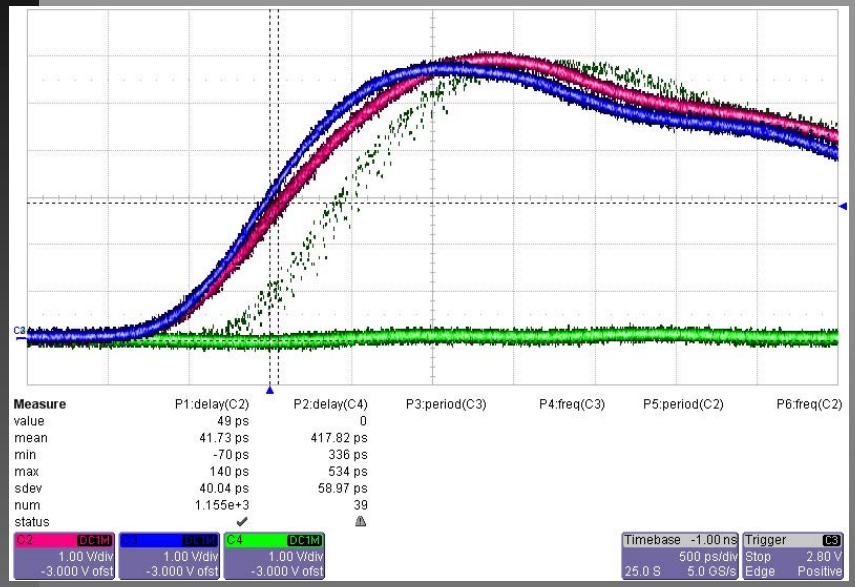
DSO – prikaz signala

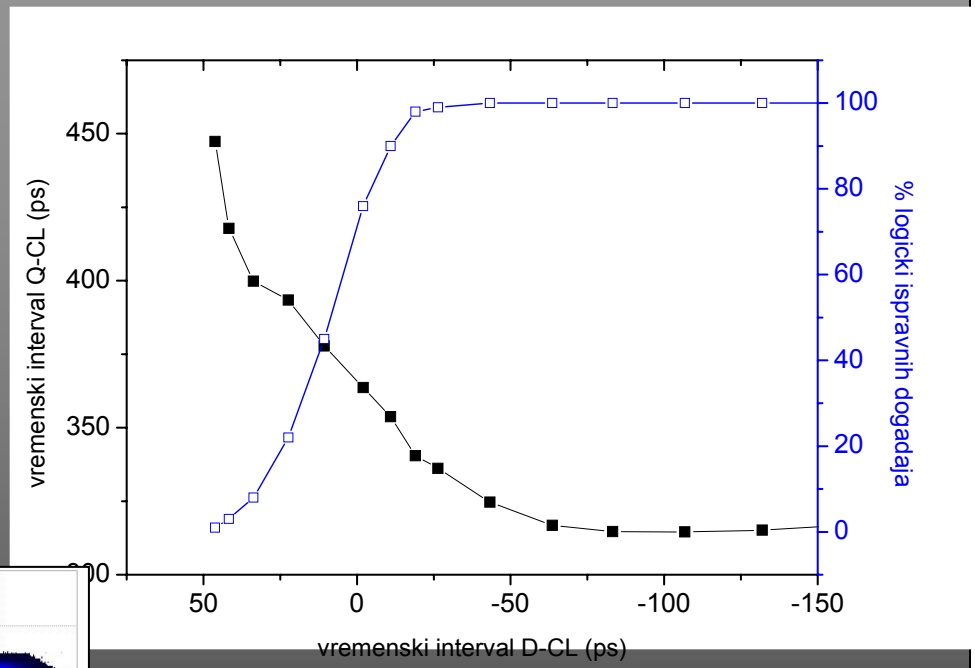
data signal (C3)
clock signal (C2)
output signal (C4)

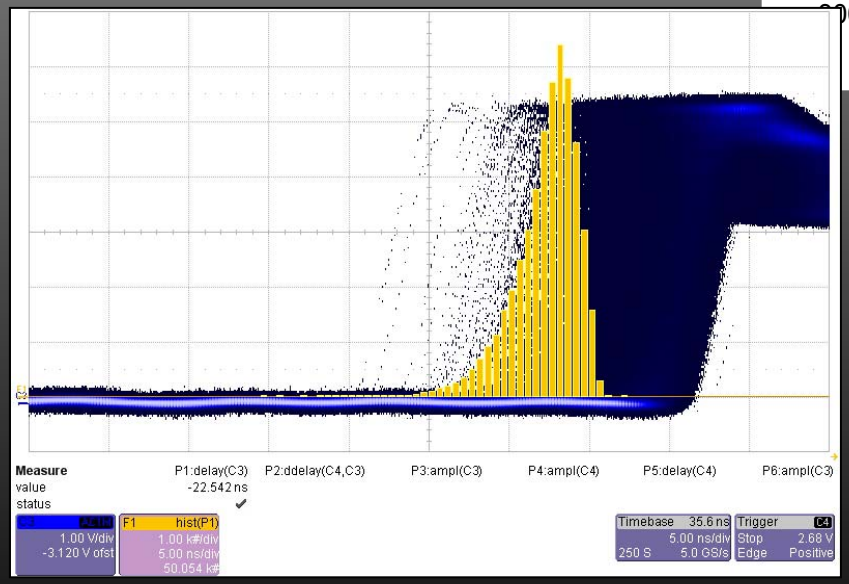


Measure	P1:time@lv(C4)	P2:time@lv(C4)	P3:time@lv(C4)	P4:time@lv(C4)	P5:time@lv(C4)	P6:ddelay(C3,C2)
value	0	0	0	0	0	14.159 ns
mean	16.07582 ns	18.43300 ns	21.17966 ns	23.60018 ns	25.57123 ns	5.86881 ns
min	14.563 ns	16.532 ns	19.106 ns	21.579 ns	24.274 ns	4.175 ns
max	27.615 ns	27.615 ns	27.615 ns	27.615 ns	27.615 ns	14.483 ns
sdev	1.41097 ns	1.85476 ns	1.88300 ns	1.63440 ns	1.00705 ns	3.17662 ns
num	4.366e+3	752	172	51	17	9.589e+3
status	⚠	⚠	⚠	⚠	⚠	✔

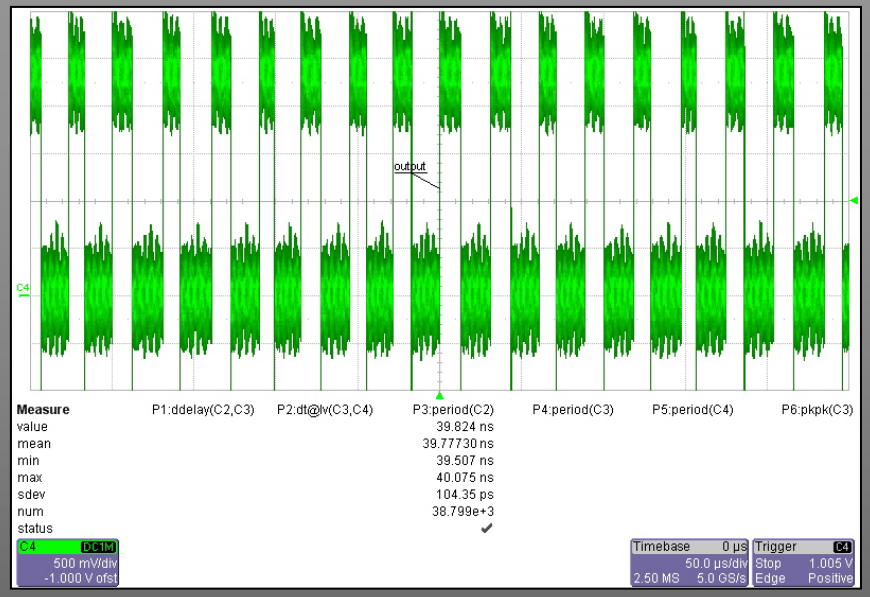
200ps

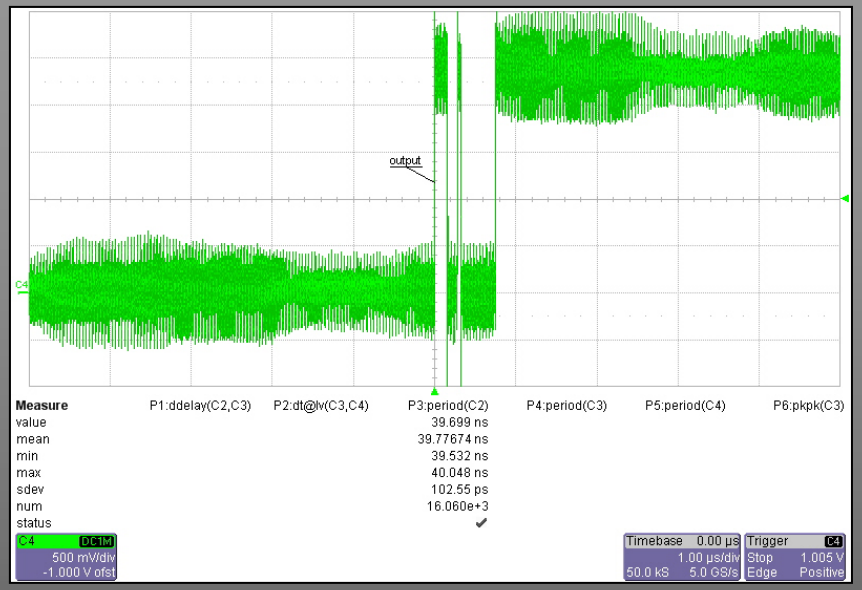


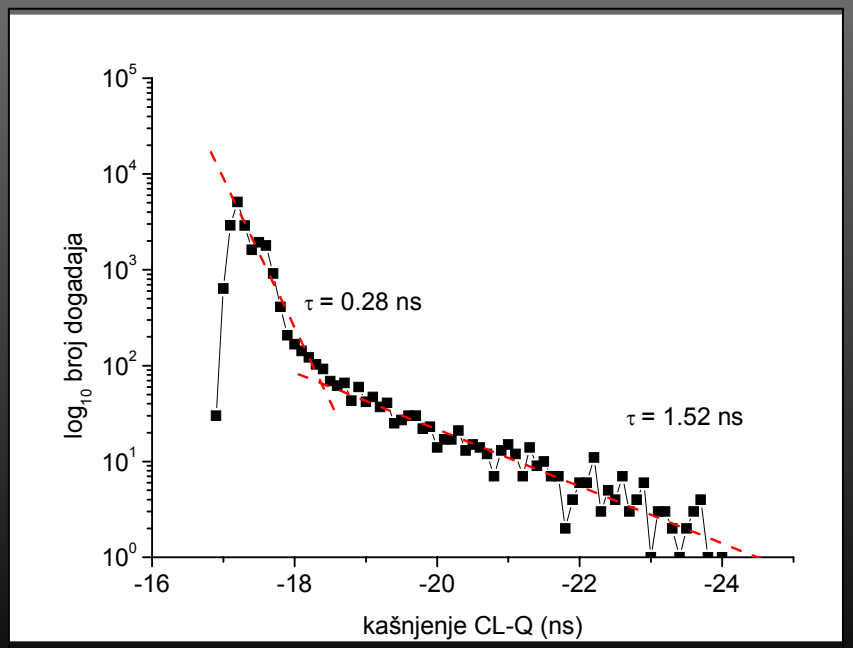




Foley metoda

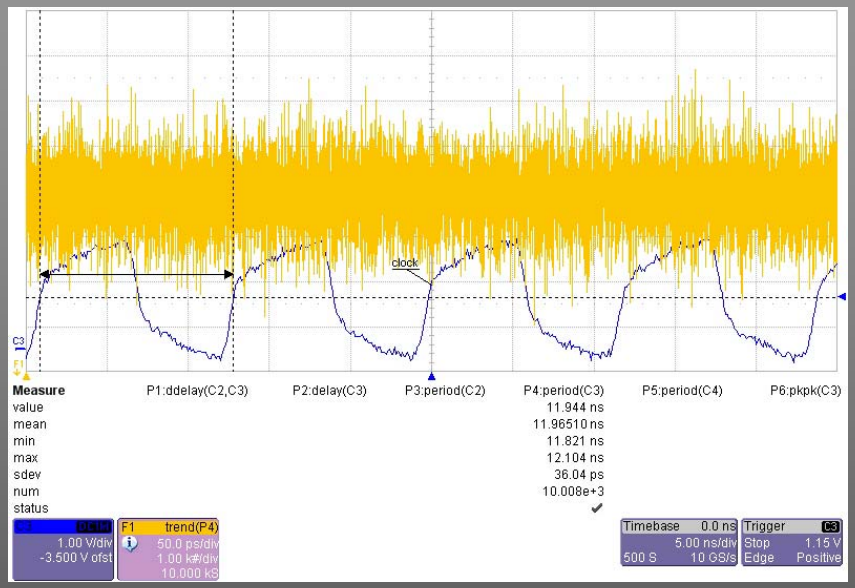


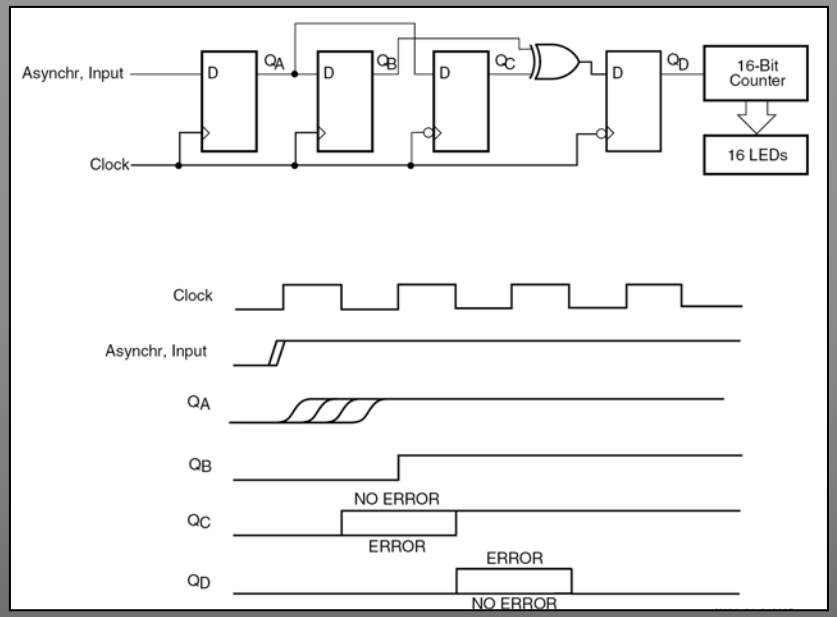




Metoda oscilatori

LTD metoda





IOB, f_D= 20.55 MHz

Frekvencija (MHz)	Poluperiod (ns)	Razlika (ps)	Broj događaja	Vrijeme (s)	MTBF (ms)
420	1.19048	-	643	60	93.3126
560	0.892857	297.619	27954	60	2.14638

τ = 0.0854 ns

Tablica 3.8: Rezultati mjerenja IOB Virtex-5 FPGA LTD metodom

Zaključak o metodama

- Metoda Foley i Metoda s oscilatorima pokazale se dovoljno razlučive, ponovljive, jednostavne i daju jednake rezultate i u slučaju brzih programirljivih tehnologija. Predstavljaju idealno rješenje za primjenu u laboratorijskim uvjetima budući da osim određivanja konstante razlučivosti i širine prozora metastabilnosti daju i mogućnost izravnog praćenja vremenskih značajki signala u uvjetima metastabilnosti.
- Nova LTD metoda i PLL za generiranje signala takta pružaju optimalne mogućnosti za realizaciju jednostavnijeg mjernog okruženja za potrebe mjerenja u industrijskim uvjetima.

Usporedba rezultata mjerenja

	Vrsta bistabila	τ (ps)	Tw (ps)	Metoda/Izvor
Spartan-3	IOB	28	<10	Foley
		40	<10	Osc
		34-38	-	LTD
	CLB	-	-	Foley
		37-39	<10	Osc
		-	-	LTD
Virtex-5	?[8]	68	-	[14]
	IOB	22	<10	Foley
		20	<10	Osc
		39	-	LTD
	CLB	63-92	<10	Foley
		65-88	<10	Osc
		129	-	LTD
ispMACH 4A	-	53	0.025	[15]
		42	$1.012 \cdot 10^{7}$	[16]
		176	nema podatka	[2]
		61	0.490 / 0.030	[2]

Tablica 4.1: Značajke metastabilnosti FPGA i CPLD bistabila

Problem metastabilnosti pri uporabi sklopovlja zasnovanog na taktom vođenim bistabilima

- ne postoji mogućnost potpune eliminacije metastabilnog ponašanja
- uporaba bržih bistabila redovito smanjuje vjerojatnost metastabilnosti
- dva ili više bistabila spojena u seriju (kvadrat vrijednosti vjerojatnosti!)
- vjerojatnost da će pojava metastabilnosti ugroziti funkcionalnost sklopa smanjuje se eksponencijalno sa smanjenjem frekvencije takta
- moderni programirljivi sklopovi su bitno pouzdaniji s obzirom na vjerojatnost metastabilnosti (nemogućnost detektiranja metastabilnostI)
- utjecaj temperature i promjena napona napajanja potrebno dodatno istražiti